ICCD 2021 Paper #4

# PSACS: Highly-Parallel Shuffle Accelerator on Computational Storage

Chen Zou<sup>1</sup>, Hui Zhang<sup>2</sup>, Yang Seok Ki<sup>2</sup>, Andrew A. Chien<sup>1,3</sup> {chenzou@, achien@cs.}uchicago.edu, {w.hzhang86, yangseok.ki}@samsung.com

<sup>1</sup>Department of Computer Science, University of Chicago <sup>2</sup> Memory Solution Lab, Samsung Semiconductor Inc. <sup>3</sup> Mathematics and Computer Science, Argonne National Laboratory



## Shuffle enables parallelism exploitation for OLAP



(v))



#### However, Shuffle may be a bottleneck



Most challenging! Cache thrashing. Spills





## Shuffle may take 1/3 latency of an OLAP query

TPC-H with scaling factor 1000.

4 nodes running Spark 3.0.1 connected with 1Gbps ethernet.

CPU time collected with JVMprofiler[6].







# PSACS: Highly-Parallel Shuffle Accelerator on Computational Storage

First shuffle acc on computational storage.

- Confines shuffle traffics in storage
- Liberates CPU and memory

PSACS microarchitecture exploits:

- Task, subtask and data-level parallelism
- Custom scratchpad for efficient gathering

PSACS achieves acceleration benefits:

- 5x kernel-level shuffle throughput
- 23% OLAP query speedup on average





## PSACS partition approach: Hash

We opt for hash-based partition for its generality.

'evenness' rather than 'collision resistance' is the key here.

We apply a variant of fold hash that additionally zig-zag the input.

b <sub>00</sub>	b <sub>01</sub>	b <sub>02</sub>	b <sub>03</sub>	b <sub>04</sub>	b <sub>05</sub>	b <sub>06</sub>	b <sub>07</sub>	b <sub>08</sub>	b <sub>09</sub>
$\oplus$									
b <sub>19</sub>	$b_{18}$	b <sub>17</sub>	$b_{16}$	$b_{15}$	$b_{14}$	$b_{13}$	$b_{12}$	$b_{11}$	$b_{10}$
$\oplus$									
b <sub>20</sub>	$b_{21}$	b <sub>22</sub>	$b_{23}$	$b_{24}$	$b_{25}$	$b_{26}$	$b_{27}$	$b_{28}$	$b_{29}$
					•				
n <sub>00</sub>	n <sub>01</sub>	n <sub>02</sub>	n <sub>03</sub>	n <sub>04</sub>	n <sub>05</sub>	n <sub>06</sub>	n <sub>07</sub>	n <sub>08</sub>	n <sub>09</sub>





# PSACS group approach

Bucketing (BypassMergeSortShuffleWriter, FPGAPart[12], Vitis[13]):

- Maintain a bucket for each destination partition to hold records going there.
- Hard to implement growable buckets without malloc-like dynamic memory allocation in hardware accelerators.
- Static bucket allocation presents linear scaling between capacity and #partitions.
- Parallelism exploitation leads to another shuffle problem.





# PSACS group approach

Bucketing (BypassMergeSortShuffleWriter, FPGAPart[12], Vitis[13]):

- Maintain a bucket for each destination partition to hold records going there.
- Hard to implement growable buckets without malloc-like dynamic memory allocation in hardware accelerators.
- Static bucket allocation presents linear scaling between capacity and #partitions.
- Parallelism exploitation leads to another shuffle problem.

Sort (SortShuffleWriter):

- : 🕐
- Sort the records by their assigned destination partition ids.
- Fixed resource requirement for different #partitions.
- Further optimization of only sorting record pointers rather than full records. Gather the records with sorted record pointers later using customized scratchpads.









FSM: Controls the shuffle process.





**FSM**: Controls the shuffle process. **Reader**: Manages a customized scratchpad as a on-chip random access buffer for the table data.





**FSM**: Controls the shuffle process. **Reader**: Manages a customized scratchpad as a on-chip random access buffer for the table data. **Partitioner**: Accepts shuffle keys streamed from the reader. Map keys via hash to partition ID (PID).





**FSM**: Controls the shuffle process. **Reader**: Manages a customized scratchpad as a on-chip random access buffer for the table data. **Partitioner**: Accepts shuffle keys streamed from the reader. Map keys via hash to partition ID (PID). **Sorter**: Sorts tuple (PID, RecPtr) from Partitioner by PID and stream the sorted tuples into Gather.





**FSM**: Controls the shuffle process. Reader: Manages a customized scratchpad as a on-chip random access buffer for the table data. **Partitioner**: Accepts shuffle keys streamed from the reader. Map keys via hash to partition ID (PID). **Sorter**: Sorts tuple (PID, RecPtr) from Partitioner by PID and stream the sorted tuples into Gather. Gather: Gathers records from Reader by RecPtrs in sorted tuple streams through random accessing.





**FSM**: Controls the shuffle process. **Reader**: Manages a customized scratchpad as a on-chip random access buffer for the table data. **Partitioner**: Accepts shuffle keys streamed from the reader. Map keys via hash to partition ID (PID). **Sorter**: Sorts tuple (PID, RecPtr) from Partitioner by PID and stream the sorted tuples into Gather. **Gather:** Gathers records from Reader by RecPtrs in sorted tuple streams through random accessing. Writer: Stream records from Gather to DRAM, handling DRAM protocol





### **PSACS** implementation



	LUT	FF	BRAM	URAM	DSP
Avail	522720	1045440	984	128	1968
Used	61917	80885	433	64	0
Util	11.85%	7.74%	44.00%	50.00%	0.00%





#### PSACS VS hand-optimized software



Single PSACS kernel VS single-thread software **5x kernel-level throughput** 





#### PSACS VS hand-optimized software



Single PSACS kernel VS single-thread software **5x kernel-level throughput** 



4-way-system pipeline with single PSACS VS 32-thread software (Data preparation and results writing back to storage included). ~20% higher system-level performance



#### CPU utilization reduction and overall query speedup





20x CPU utilization reduction

23% end-to-end query speedup on average



#### **Related work**

**Single-node partition acceleration:** Both academia[12] and industry[13]. Bucketbased grouping for single-node is used.

**Specific function acceleration in OLAP**: Cereal[23] accelerates serialization, SortAcc[14] accelerates sorting, CASM[15] accelerates local aggregation.

**Network fabric improvement**: SparkRDMA[10], SparkPMoF[11].

**Software optimization for shuffle**: Riffe[8] optimizes storage IO and network transfer with special merge policy. Intel proposes in-memory shuffle[24] in a disaggregated optane pool.





## Summary

We proposed PSACS, the first shuffle accelerator addressing the shuffle bottlenecks of the OLAP systems.

- Employs rising computational storage paradigm
- Hardware acceleration through exploitation of multiple levels of parallelism
- Utilizes custom scratchpad for high-speed gathering

PSACS delivers 5x throughput at the kernel level and on average 23% end-to-end OLAP query speedup.

See our paper for more PSACS features

- Tiled shuffling tailoring for different levels inside the memarch
- Column-major output for higher compression ratio during fetch

